Assignment 4: Question 4.2

\* Project : Assignment 4

\* Name of the file : COA\_A4\_P2

\* Brief Description of file : Assembly code to implement a triple layered page table and illustrate protection

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The page table has been created to identically map the virtual address to physical address and this automatically starts Page 1. The linker loads the code at 0x10010000 and we use this knowledge to set page table accordingly.

We first load sp value, machine trap handler and supervisor trap handler addresses.

Following the address calculations and right shift as mentioned in the RISC V specifications, we set pmp addresses and pmp configuration values, which enables the physical memory protection, i.e. pmp. This is done similar to what was done in Question 4.1, however with pages of size 4 kB.

After this, we switch privilege levels from machine to supervisor mode, wherein we set satp with the root page table address and mode, again similar to Question 4.1.

We implement the three layered page table and also delegate instruction access fault to supervisor mode for illustration of protection.

Page 2:

We show that the machine mode code is inaccessible from supervisor mode by attempting and failing to jump from supervisor to machine mode thus causing an instruction access fault, as the supervisor mode code is accessible from both levels whereas machine mode code is only accessible from machine mode, once again, similar to Question 4.1, as seen when a1 becomes 1.

We also illustrate page miss which is seen when a0 value becomes 12.

Page 3:

We illustrate page miss by setting faulty page entry for second page.

The specifics of which functionality of the above explanation is done and where is shown via comments in the assembly code file.